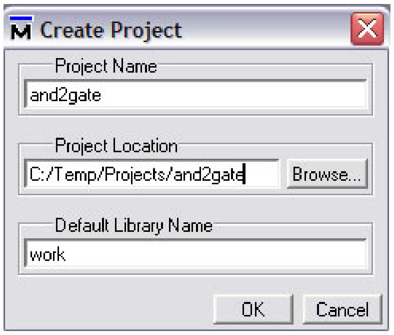
ModelSim SE 6.1b Tutorial

1. Start ModelSim
2. Create a new project
   - Click on *File*, then *New*, then choose *Project* on the drop down menu
   - Enter your project name, in this case the project is called “and2gate”
   - Choose your project location, this project is stored at “C:\Temp\Projects\and2gate”
   - The default library name should be *work*.
   - Click *OK* button

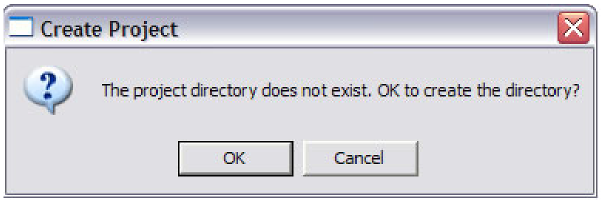


Project Name: and2gate

Project Location: C:/Temp/Projects/and2gate

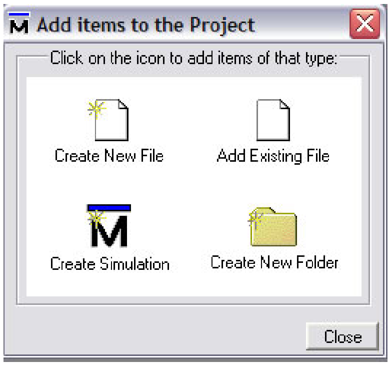
Default Library Name: work

3. You will be asked if want to create the project directory.
   - Click *OK* button



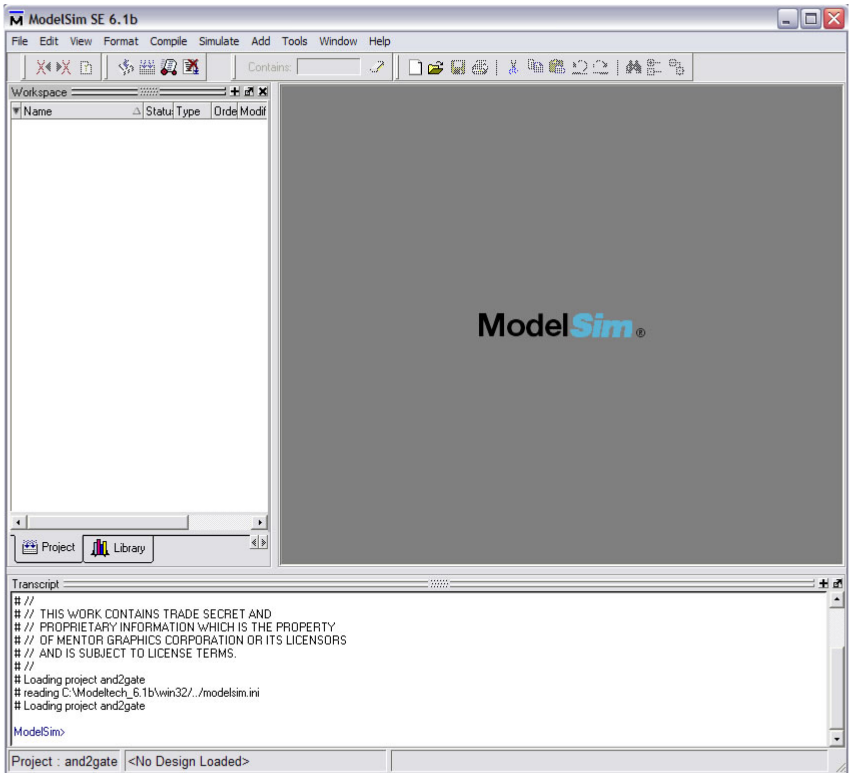
The project directory does not exist. OK to create the directory?

4. Next you will be presented with the Add Items to Project Dialog. While you can use this dialog to create new source files of add existing ones, we will not be using this option for the tutorial. We’ll add source files later so just click on the *Close* button



Click on the icon to add items of that type:

5. You now have a project by the name of “and2gate”.

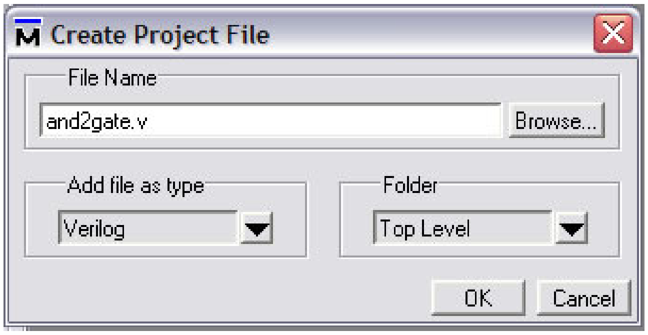

ModelSim SE 6.1b
File Edit View Format Compile Simulate Add Tools Window Help
Contains:
Workspace
Name Statu Type Orde Modif
Project
Library
ModelSim
Transcript

```
# //
# //  THIS WORK CONTAINS TRADE SECRET AND
# //  PROPRIETARY INFORMATION WHICH IS THE PROPERTY
# //  OF MENTOR GRAPHICS CORPORATION OR ITS LICENSORS
# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading project and2gate
# reading C:\Modeltech_6.1b\win32/../modelsim.ini
# Loading project and2gate

ModelSim>
```

Project : and2gate <No Design Loaded>

6. Now we want to add a new file to our project.
- Click on *File*, choose *Add to Project*, and choose *New File…*
- Choose *Verilog* as the file type
- In the *File name:* box enter the desired file name, in this case the file is named “and2gate.v”
- Click on the *OK* button

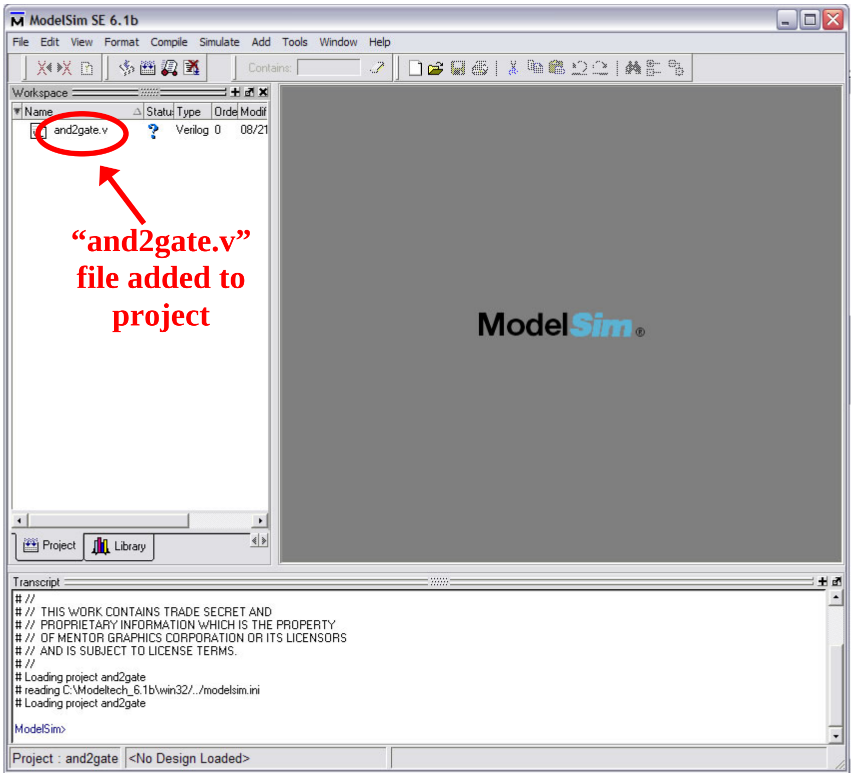


File Name: and2gate.v

Add file as type: Verilog

Folder: Top Level

7. The “and2gate.v” file has been added to your project.



“and2gate.v” file added to project

```
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# //
# Loading project and2gate
# reading C:\Modeltech_6.1b\win32/../modelsim.ini
# Loading project and2gate

ModelSim>
```
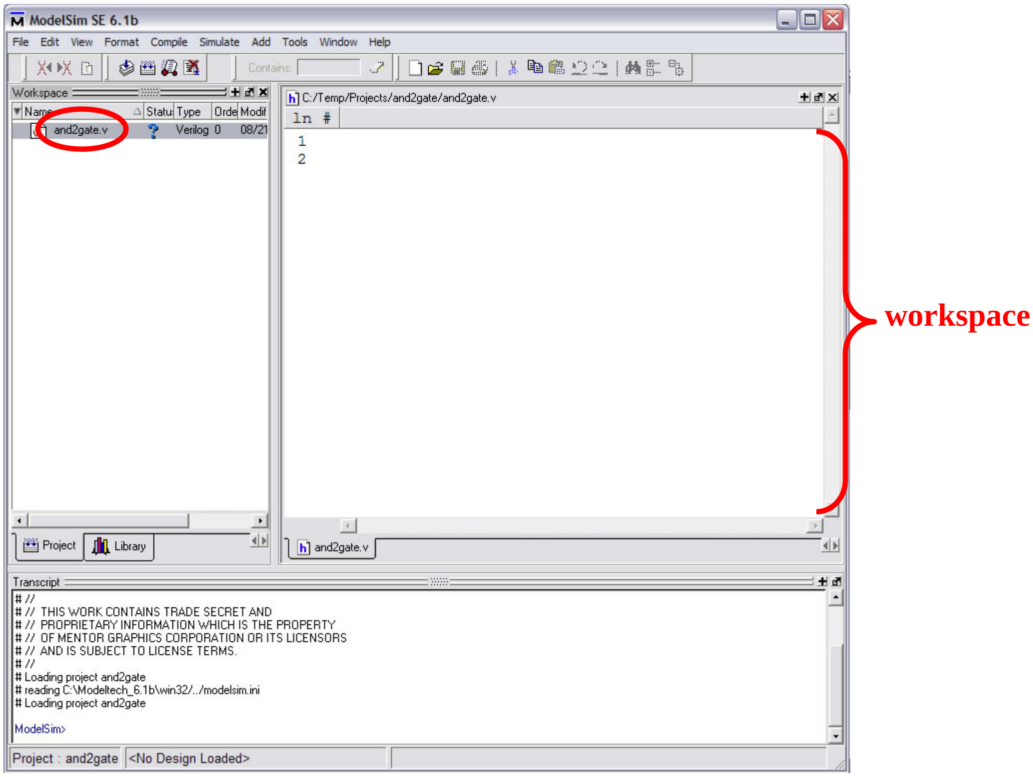

8. Double-click on the and2gate.v to show the file contents. You are now ready to specify the and2gate module’s functionality.



workspace

```
# //
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# //
# Loading project and2gate
# reading C:\Modeltech_6.1b\win32/../modelsim.ini
# Loading project and2gate

ModelSim>
```
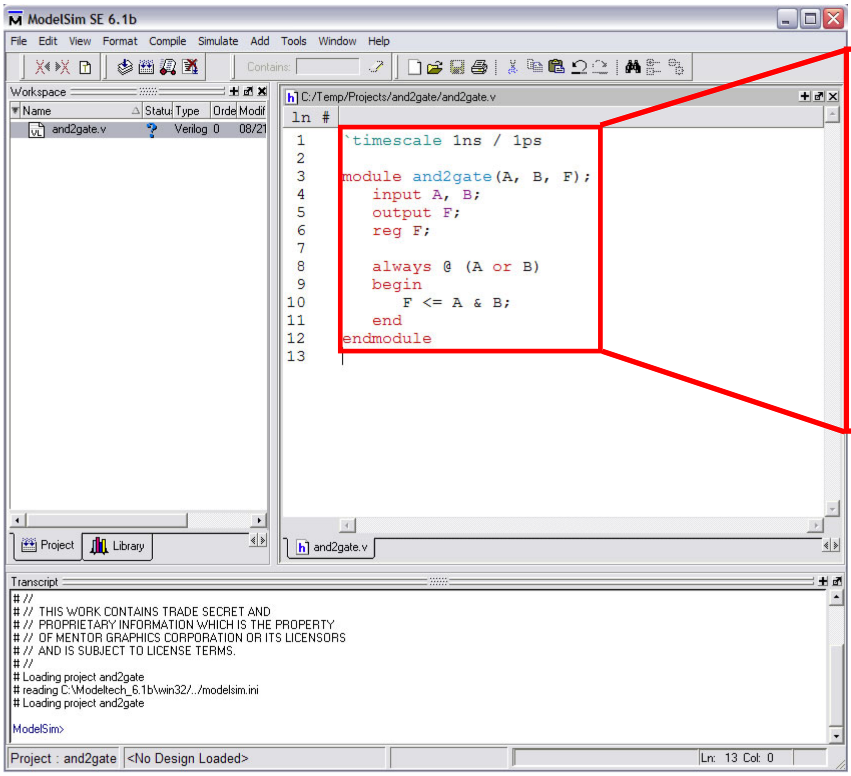

9. We compete the and2gate specification as shown below..
   - The line "`timescale 1ns/ 1ps" is located at the top of the file. The Verilog language uses dimensionless time units, and these time units are mapped to "real" time units within the simulator. `timescale is used to map to the "real" time values using the statement `timescale <time1> / <time2>, where <time1> indicates the time units associated with the #delay values, and the <time2> indicates the minimum step time used by the simulator. ***Note:*** Be sure to use the correct ` character. The ` is the not the single quotation mark (') and is typically located on the same key as the ~. If you have errors in your file, this may be the culprit.
   - The and2gate module is also declared using "module and2gate();" and "endmodule", but the ports are left for us to define.
   - Be sure to save the changes to the and2gate.v file by clicking on *File* and choosing *Save*.


ModelSim SE 6.1b
File Edit View Format Compile Simulate Add Tools Window Help
Workspace
Name Statu Type Orde Modif
and2gate.v ? Verilog 0 08/21
Project Library
C:/Temp/Projects/and2gate/and2gate.v
ln #
and2gate.v
Transcript

```
`timescale 1ns / 1ps

module and2gate(A, B, F);
        input A, B;
        output F;
        reg F;

        always @ (A or B)
        begin
                F <= A & B;
        end
endmodule
```

```
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# //
# Loading project and2gate
# reading C:\Modeltech_6.1b\win32/../modelsim.ini
# Loading project and2gate

ModelSim>
```
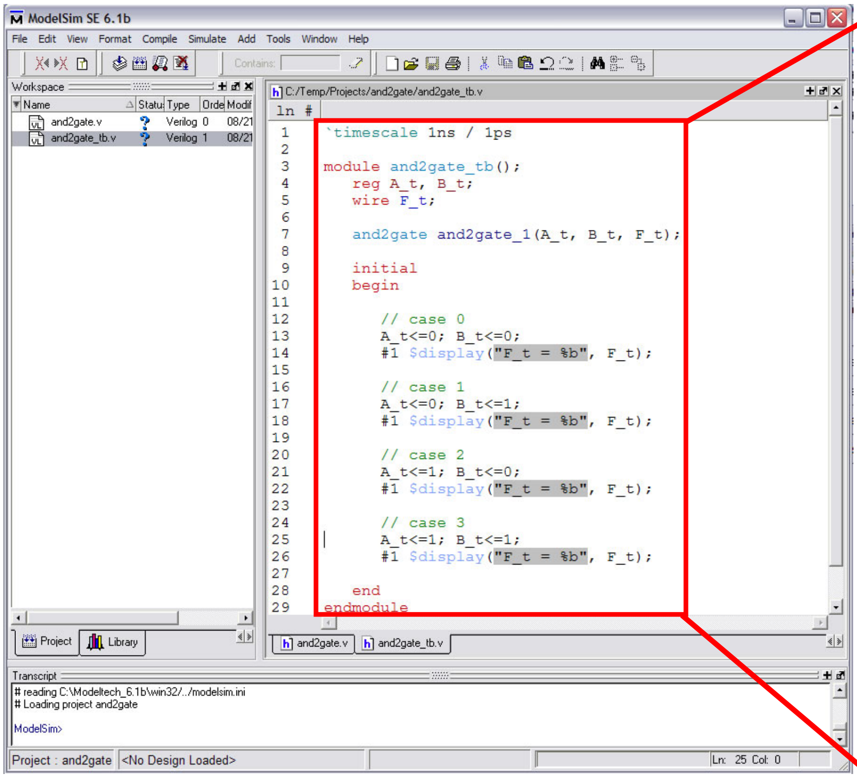

Project : and2gate <No Design Loaded> Ln: 13 Col: 0

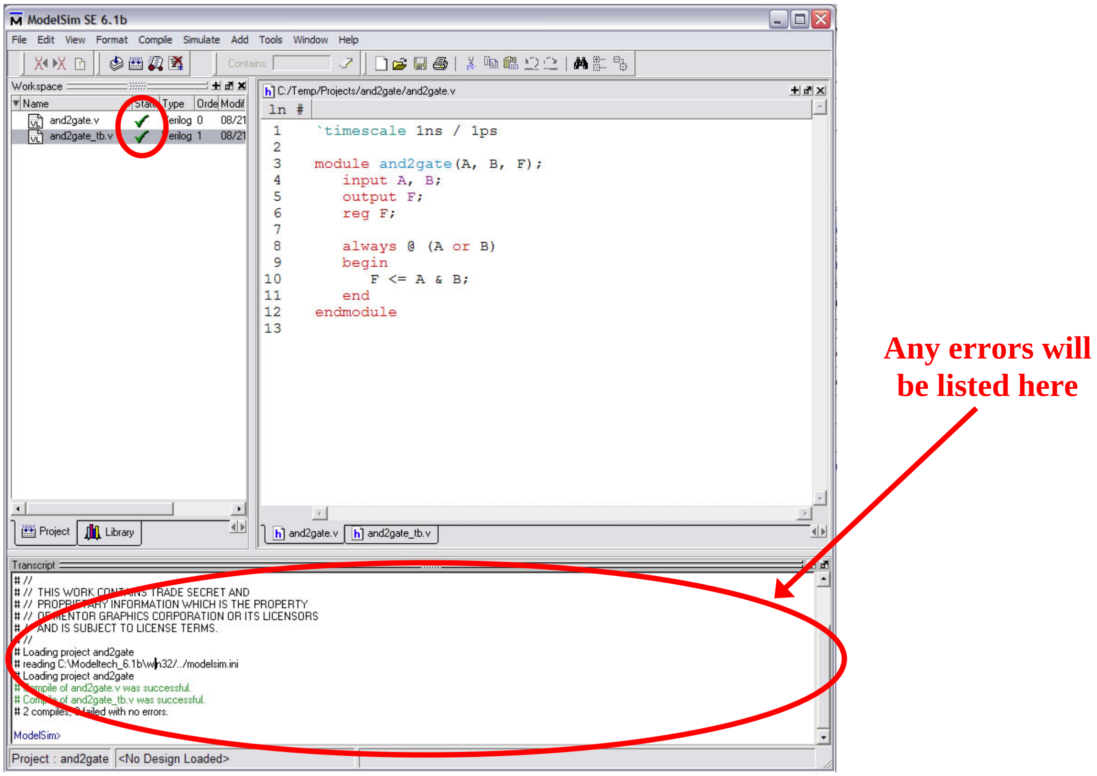
10. We also want to add a testbench and again follow Steps 6 – 9 to add “and2gate_tb.v”. Then we add the functionality of the testbench module as shown below.


ModelSim SE 6.1b
File Edit View Format Compile Simulate Add Tools Window Help
Workspace
Name Status Type Order Modif
and2gate.v ? Verilog 0 08/21
and2gate_tb.v ? Verilog 1 08/21
C:/Temp/Projects/and2gate/and2gate_tb.v
Project Library
and2gate.v and2gate_tb.v
Transcript
Project : and2gate <No Design Loaded>
Ln: 25 Col: 0

```
# reading C:\Modeltech_6.1b\win32/../modelsim.ini
# Loading project and2gate

ModelSim>
```

```
`timescale 1ns / 1ps

module and2gate_tb();
   reg A_t, B_t;
   wire F_t;

   and2gate and2gate_1(A_t, B_t, F_t);

   initial
   begin

      // case 0
      A_t<=0; B_t<=0;
      #1 $display("F_t = %b", F_t);

      // case 1
      A_t<=0; B_t<=1;
      #1 $display("F_t = %b", F_t);

      // case 2
      A_t<=1; B_t<=0;
      #1 $display("F_t = %b", F_t);

      // case 3
      A_t<=1; B_t<=1;
      #1 $display("F_t = %b", F_t);

   end
endmodule
```

11. After saving both “and2gate.v” and “and2gate_tb.v”, we want to check the syntax of both files.
    - Click on the *Compile* Menu and select *Compile All*
    - If the syntax was correct, a checkmark will appear next to each file
    - If the syntax was incorrect, the window at the bottom will list the individual errors.


ModelSim SE 6.1b
File Edit View Format Compile Simulate Add Tools Window Help
Contains:
Workspace
C:/Temp/Projects/and2gate/and2gate.v
Project
Library
and2gate.v
and2gate_tb.v
Transcript

Name	Stat	Type	Orde	Modif
and2gate.v	✓	Verilog	0	08/21
and2gate_tb.v	✓	Verilog	1	08/21

```
`timescale 1ns / 1ps

module and2gate(A, B, F);
   input A, B;
   output F;
   reg F;

   always @ (A or B)
   begin
      F <= A & B;
   end
endmodule

```

```
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# //  AND IS SUBJECT TO LICENSE TERMS.
# //
# Loading project and2gate
# reading C:\Modeltech_6.1b\win32/../modelsim.ini
# Loading project and2gate
# Compile of and2gate.v was successful.
# Compile of and2gate_tb.v was successful.
# 2 compiles, 0 failed with no errors.

ModelSim>
```
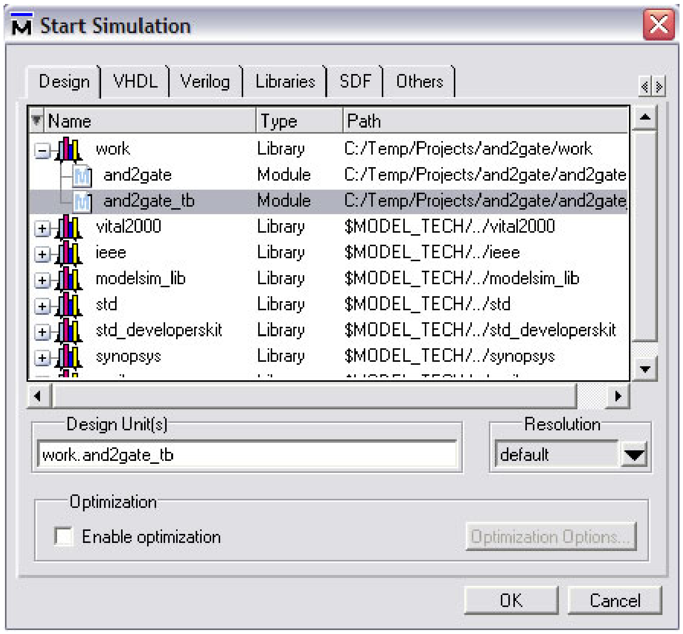

Project : and2gate   <No Design Loaded>

Any errors will be listed here

12. Now it’s time to simulate the design.
    - Click on the *Simulate* menu and choose *Start Simulation*
    - Expand the selection for the work library by click on the + symbol on the left.
    - Select and2gate_tb and click OK button



Name	Type	Path
work	Library	C:/Temp/Projects/and2gate/work
and2gate	Module	C:/Temp/Projects/and2gate/and2gate
and2gate_tb	Module	C:/Temp/Projects/and2gate/and2gate
vital2000	Library	$MODEL_TECH/../vital2000
ieee	Library	$MODEL_TECH/../ieee
modelsim_lib	Library	$MODEL_TECH/../modelsim_lib
std	Library	$MODEL_TECH/../std
std_developerskit	Library	$MODEL_TECH/../std_developerskit
synopsys	Library	$MODEL_TECH/../synopsys

Design Unit(s): work.and2gate_tb

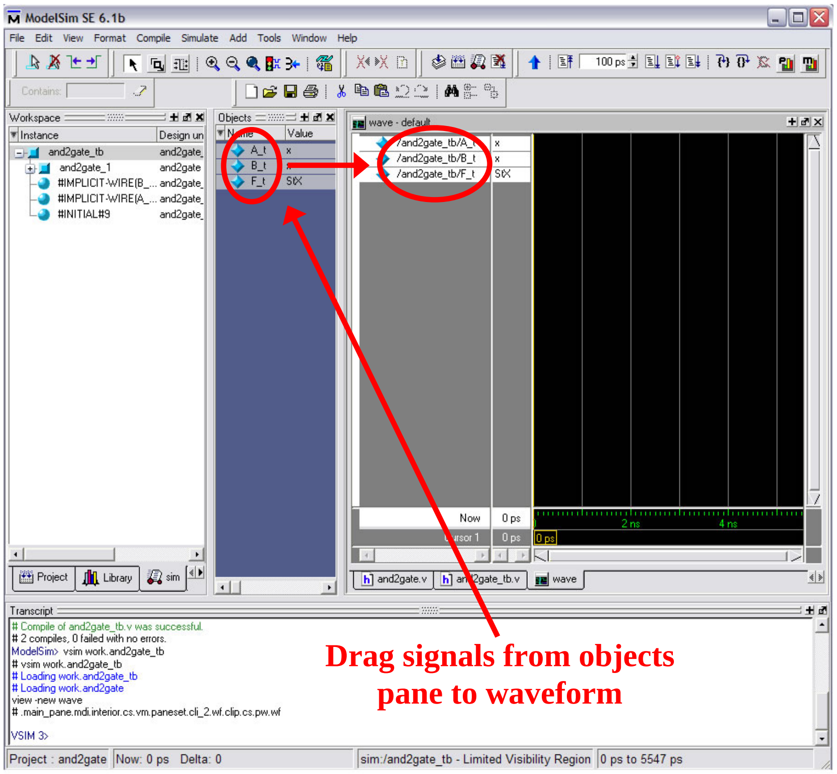
Resolution: default

Optimization

□ Enable optimization

Optimization Options...

13. Next we create a simulation waveform window.
    - Click on *File* menu, choose *New*, then choose *Windows*, then choose *Wave*
    - Add the signals that would like to monitor by dragging the signal from the middle pane to the waveform window as shown below

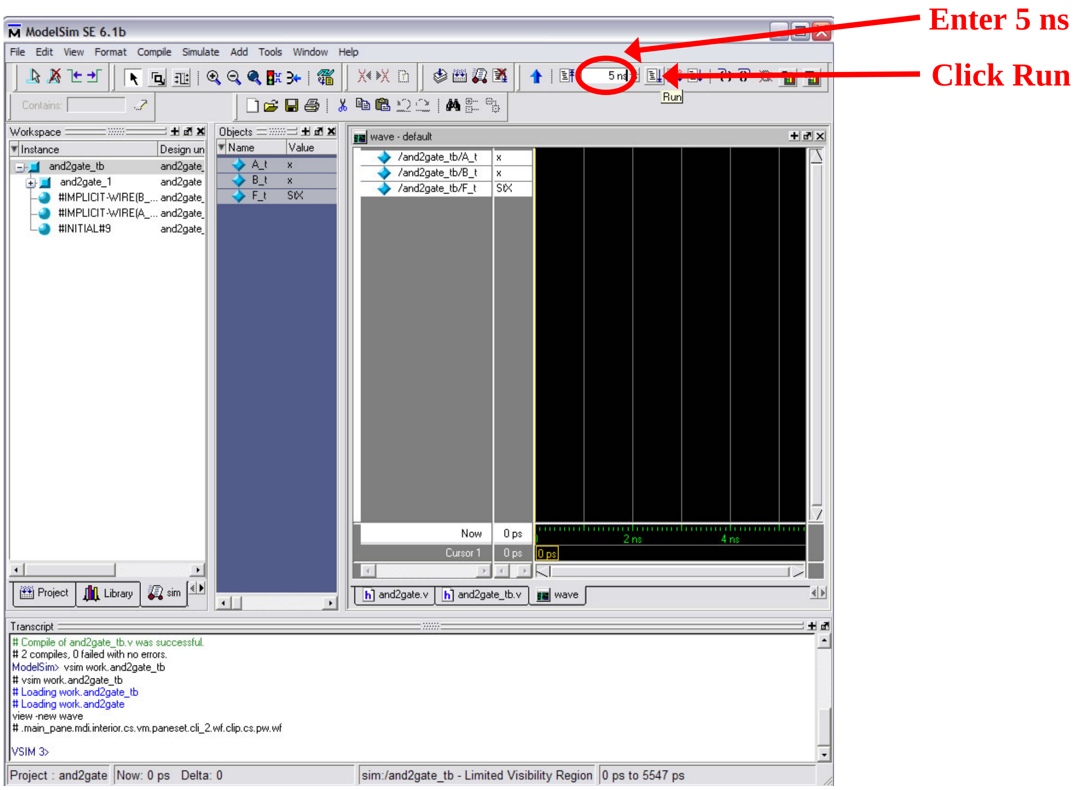


```
# Compile of and2gate_tb.v was successful.
# 2 compiles, 0 failed with no errors.
ModelSim> vsim work.and2gate_tb
# vsim work.and2gate_tb
# Loading work.and2gate_tb
# Loading work.and2gate
view -new wave
# .main_pane.mdi.interior.cs.vm.paneset.cli_2.wf.clip.cs.pw.wf

VSIM 3>
```

Project : and2gate | Now: 0 ps Delta: 0 | sim:/and2gate_tb - Limited Visibility Region | 0 ps to 5547 ps

Drag signals from objects pane to waveform

14. We can simulate the design.
    - Enter 5 ns as the length of time we would like to simulate for in the Run Length box and click the Run icon as shown below.



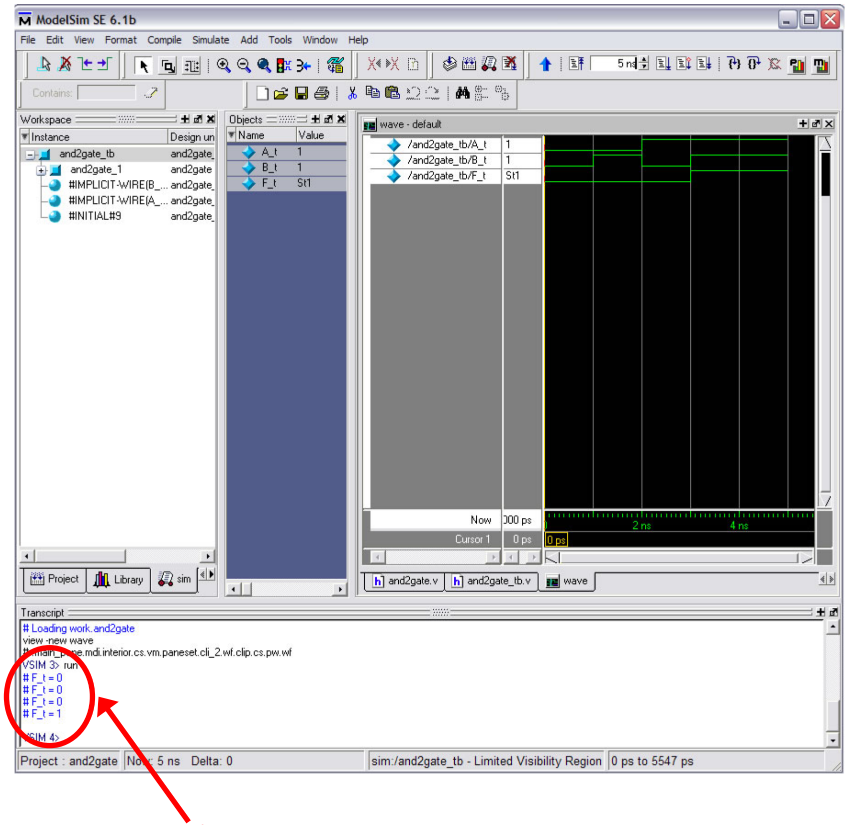
Enter 5 ns

Click Run

```
# Compile of and2gate_tb.v was successful.
# 2 compiles, 0 failed with no errors.
ModelSim> vsim work.and2gate_tb
# vsim work.and2gate_tb
# Loading work.and2gate_tb
# Loading work.and2gate
view -new wave
# .main_pane.mdi.interior.cs.vm.paneset.cli_2.wf.clip.cs.pw.wf

VSIM 3>
```

Project : and2gate | Now: 0 ps Delta: 0 | sim:/and2gate_tb - Limited Visibility Region | 0 ps to 5547 ps

15. Our simulation is complete. The simulation waveforms appear and we can check the and2gate module's functionality. Further, the $display statements included in the testbench appear in the lower window.



Instance	Design un
and2gate_tb	and2gate_
and2gate_1	and2gate
#IMPLICIT-WIRE(B_...	and2gate_
#IMPLICIT-WIRE(A_...	and2gate_
#INITIAL#9	and2gate_

Name	Value
A_t	1
B_t	1
F_t	St1

/and2gate_tb/A_t	1
/and2gate_tb/B_t	1
/and2gate_tb/F_t	St1
Now	000 ps
Cursor 1	0 ps

```
# Loading work.and2gate
view -new wave
#.main_pane.mdi.interior.cs.vm.paneset.cli_2.wf.clip.cs.pw.wf
VSIM 3> run
# F_t = 0
# F_t = 0
# F_t = 0
# F_t = 1

VSIM 4>
```

Project : and2gate   Now: 5 ns   Delta: 0   sim:/and2gate_tb - Limited Visibility Region   0 ps to 5547 ps

$display statements appear here